

Appl. No. 10/666,570

Dated 11/23/2004

Reply to Office Action of 10/26/2004

IN THE CLAIMS

Please amend claims 15-16 as follows below.

Please cancel claims 23-29 without prejudice.

Please add new claims 30-32 as follows below.

MARKED UP VERSION OF CLAIMS

1           1-13. (Cancelled)

1           14. (Original) An instruction set architecture (ISA)  
2   for execution of operations within a digital signal processor,  
3   the instruction set architecture comprising:  
4                a set of instructions for operation within a  
5                digital signal processor wherein each instruction  
6                includes a first operand accessed directly from memory,  
7                a second operand accessed directly from memory of a  
8                local register, and a destination register to store  
9                results, the set of instructions including,  
10               a 20-bit DSP instruction, and  
11               a 40-bit DSP instruction,  
12               the set of instructions to accelerate  
13               calculations within the digital signal processor of  
14               the type where  $D = [ (A \text{ operation one } B) \text{ operation}$   
15               two  $C ]$  where operation one and operation two are  
16               separate signal processing operations.

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1           15. (Currently Amended) The instruction set architecture  
2 (ISA) of claim 14 for execution of operations within a digital  
3 signal processor, wherein,  
4           the twenty bit instruction uses mode bits in control  
5 registers ~~(i.e. mode registers)~~ and the forty bit instruction  
6 has a control extension to override the mode bits.

1           16. (Currently Amended) An ~~[[The]]~~ instruction set  
2 architecture (ISA) ~~of claim 14~~ for execution of operations  
3 within a digital signal processor, ~~wherein, the set of~~  
4 ~~instructions further includes the instruction set architecture~~  
5 comprising:  
6                   a set of instructions for operation within a  
7                   digital signal processor wherein each instruction  
8                   includes a first operand accessed directly from memory,  
9                   a second operand accessed directly from memory of a  
10                   local register, and a destination register to store  
11                   results, the set of instructions including,  
12                   a 20-bit DSP instruction,  
13                   a 40-bit DSP instruction, and  
14                   a dyadic instruction to execute two operations  
15                   in one instruction;  
16                   the set of instructions to accelerate  
17                   calculations within the digital signal processor of the

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18           type where D = [ (A operation one B) operation two C ]  
19           where operation one and operation two are separate  
20           signal processing operations.

1           17. (Original) The instruction set architecture (ISA)  
2 of claim 16 for execution of operations within a digital  
3 signal processor, wherein  
4           the two operations of the dyadic instruction for  
5 execution in one instruction are DSP operations.

1           18. (Original) The instruction set architecture (ISA)  
2 of claim 17 for execution of operations within a digital  
3 signal processor, wherein  
4           the DSP operations are of the set of operations of  
5 multiplication, addition, extremum, and no operation.

1           19-20. (Cancelled).

1           21. (Previously Presented) The instruction set  
2 architecture (ISA) of claim 15 for execution of operations  
3 within a digital signal processor, wherein,  
4           the control registers are mode registers.

1           22-29. (Cancelled)

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1        30. (New) The instruction set architecture (ISA) of  
2 claim 14 for execution of operations within a digital signal  
3 processor, wherein

4        the digital signal processing operations are of the set  
5 of operations of multiplication, addition, extremum, and no  
6 operation.

1        31. (New) The instruction set architecture (ISA) of  
2 claim 16 for execution of operations within a digital signal  
3 processor, wherein,

4        the twenty bit instruction uses mode bits in control  
5 registers and the forty bit instruction has a control  
6 extension to override the mode bits.

1        32. (New) The instruction set architecture (ISA) of  
2 claim 31 for execution of operations within a digital signal  
3 processor, wherein,

4        the control registers are mode registers.